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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,920	10/30/2003	Jung Pill Kim	2003P52789US	8247

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,920	KIM ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-13* is/are allowed.

6)☒ Claim(s) *1,2,5-7,14,16-18,20,22 and 24-27* is/are rejected.

7)☒ Claim(s) *3,4,15,19, 21 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-27 are presented in the instant application according to the Applicants' filing on 10/30/2003.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 22, 24, 25, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Katoh (U.S. Patent No. 6,252,465).

With respect to claims 1 and 22, Katoh discloses, in Figure 3, a phase blending circuit and a corresponding method for generating a plurality of signals differing in phase relative to an early phase signal comprising a) a current source [top transistor of box 28] having a common output node [common node of drains of transistors in box 28]; b) one or more delay elements

[inverter in box 27], and c) one or more switches [first and bottom transistors of box 27] to selectively couple one or more of the delay elements to the common output node of the current source, wherein a time required for a voltage level at the common output node to fall below a threshold level after assertion of the early phase signal is dependent on which of the one or more delay elements are coupled to the common output node.

With respect to claims 2 and 24, Katoh discloses, in Figure 3, that the one or more delay elements comprises at least one transistor [middle transistors] to provide a path for current flow from the common output node of the current source in response to assertion of the early phase signal.

With respect to claim 25, Katoh discloses, in Figure 3, that the one or more switches comprise one or more transistors [top and bottom transistors of box 27].

With respect to claim 27, Katoh discloses, in Figure 3, that the late signal trails the early signal by a unit delay; and the switches [top and bottom transistors of box 27] and delay elements [middle two transistors of box 27] are configured to provide the delayed signal differing in phase from the early signal by a fraction of the unit delay, wherein the fraction depends on which of the switches are closed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-7 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh (U.S. Patent No. 6,252,465) in view of Saeki (U.S. Patent No. 6,388,490).

With respect to claim 5-7 and 26, Katoh discloses all of the claimed limitations as expressly recited in claim 1, including one or more delay elements coupled with the common output node of the current source, except for a) the one or more delay elements comprises at least one capacitor, b) the at least one capacitor comprises a plurality of capacitors having different values of capacitance, and c) the capacitor values are selected such that the phases of the plurality of signals are separated by a substantially equal phase.

Saeki discloses, in Fig. 3, a delay circuit including delay elements comprises at least one capacitor, b) the at least one capacitor comprises a plurality of capacitors having different values of capacitance [16C, 8C, 4C, 2C, C], and c) the capacitor values are selected such that the phases of the plurality of signals are separated by a substantially equal phase.

To configure the circuit of Katoh with a delay circuit, having a plurality of capacitors of different values selected in a way such that the phase of the signals are separated by an equal phase as taught by Saeki to broaden the operating range of phase adjustment would have been obvious to one of ordinary skill in the art at the time of the invention since Saeki teaches that this particular delay circuit would provide the capability of allowing performing coarse period adjustment in advance *(see Saeki, col. 2, lines 1-7).*

6. Claims 14 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (Fig. 1) in view of Katoh (U.S. Patent No. 6,252,465).

With respect to claims 14 and 16-17, Applicant Admitted Prior Art discloses, in Fig. 1, a delay locked loop circuit for generating an output signal aligned with an input signal comprising

a) a delay line [102] for providing phase signals delayed relative to the input signal [CK in] by one or more of unit delays, b) a phase blending circuit [108] for generating a blended phase signal and c) control logic configured to monitor skew between the input and output signals and, based on the skew, generate one or more control signals to select the early and late signals provided to the phase blending circuit and to selectively couple one or more of the delay elements to a common output node.

Applicant Admitted Prior Art fails to disclose a specific configuration of the claimed phase blending circuit including a current source having a common output node, one or more delay elements, one or more switches to selectively couple one or more of the delay elements to the common output node of the current source, wherein a time required for a voltage level at the common output node to fall below a threshold level after assertion of the early phase signal is dependent on which of the one or more delay elements are coupled to the common output node, a comparator having an input node coupled with the common output node of the current source, and the threshold level is the threshold level of the comparator and the output signal is generated on an output node of the comparator.

Katoh discloses, in Fig. 3, a phase blending circuit for generating a plurality of signals differing in phase relative to an early phase signal comprising a) a current source [top transistor of box 28] having a common output node [common node of drains of transistors in box 28]; b) one or more delay elements [inverter in box 27], c) one or more switches [first and bottom transistors of box 27] to selectively couple one or more of the delay elements to the common output node of the current source, wherein a time required for a voltage level at the common output node to fall below a threshold level after assertion of the early phase signal is dependent

on which of the one or more delay elements are coupled to the common output node, d) a comparator [11] having an input node coupled with the common output node of the current source, and the threshold level is the threshold level of the comparator and e) the output signal is generated on an output node of the comparator.

To configure the circuit of Applicant Admitted Prior Art, Fig. 1, with a phase blending circuit with a specific detailed description as addressed above and taught by Katoh to provide synchronization between the input signal and the reference clock would have been obvious to one of ordinary skill in the art at the time of the invention since Katoh teaches that the phase blending circuit is used for maintaining clocks input to a plurality of circuits in an integrated circuit in synchronization *(see Katoh, col. 1, lines 25-27).*

7. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwak (U.S. Patent No. 6,646,939) in view of Applicant Admitted Prior Art (Fig. 1) and Katoh (U.S. Patent No. 6,252,465).

With respect to claim 18, Kwak discloses, in Fig. 1, a dynamic random access memory (DRAM) device comprising a) one or more memory elements [60,70]; and b) a delay locked loop circuit [20] for synchronizing data output from the one or more memory elements with a clock signal.

Kwak fails to disclose a detailed description of the delay locked loop including (a) a delay line, (b) a phase blending circuit comprising a current source and one or more delay elements for selectively coupling to a common output node of the current source, in which a time required for a voltage level at the common output node to fall below a threshold level after

assertion of an early phase signal provided by the delay line is dependent on which of the one or more delay elements are coupled to the common output node, and (c) control logic configured to monitor skew between the input and output signals and, based on the skew, generate one or more control signals to select the early signal provided to the phase blending circuit by the delay line and to selectively couple one or more of the delay elements to the common output node.

Applicant Admitted Prior Art, Fig. 1, discloses a delay locked loop including (a) a delay line, (b) a phase blending circuit, and (c) control logic configured to monitor skew between the input and output signals and, based on the skew, generate one or more control signals to select the early signal provided to the phase blending circuit by the delay line and to selectively couple one or more of the delay elements to the common output node.

Applicant Admitted Prior Art, Fig. 1, lacks to disclose details of the phase blending circuit.

Katoh discloses a phase blending circuit comprising a current source and one or more delay elements for selectively coupling to a common output node of the current source, in which a time required for a voltage level at the common output node to fall below a threshold level after assertion of an early phase signal provided by the delay line is dependent on which of the one or more delay elements are coupled to the common output node.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the circuit of Kwak with a delay locked loop as taught in Applicant Admitted Prior Art, Fig. 1, including a) a delay line, b) a phase blending circuit and c) a control logic to provide sufficient synchronization between the input clock signal and the output clock signal since such

circuit arrangement of the logic circuit for the stated purpose has been a well known practice as evidenced by the teachings of Applicant Admitted Prior Art, Fig. 1 *(see Specification, [0003]).*

Furthermore, to configure the circuit of the combination of Kwak and Applicant Admitted Prior Art (Fig. 1) with a phase blending circuit, as taught by Katoh with all the details indicated in the previous paragraph, to maintain synchronization between the input signal and the reference clock would have been obvious to one of ordinary skill in the art at the time of the invention since Katoh teaches that the phase blending circuit is used for maintaining clocks input to a plurality of circuits in an integrated circuit in synchronization *(see Katoh, col. 1, lines 25-27).*

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwak (U.S. Patent No. 6,646,939) in view of Applicant Admitted Prior Art (Fig. 1) and in view of Katoh (U.S. Patent No. 6,252,465) and further in view of Saeki (U.S. Patent No. 6,388,490).

With respect to claim 20, the combination of Kwak, Applicant Admitted Prior Art (Fig. 1) and Katoh discloses all the claimed limitations as expressly recited in claim 18 above, except for the one or more delay elements comprise a plurality of capacitors.

Saeki discloses, in Fig. 3, a delay circuit including delay elements comprises at least one capacitor and the at least one capacitor comprises a plurality of capacitors having different values of capacitance [16C, 8C, 4C, 2C, C].

To configure the circuit with the combined teachings of Kwak, Applicant Admitted Prior Art and Katoh with a delay circuit including delay elements comprises at least one capacitor and the at least one capacitor comprises a plurality of capacitors having different values of

capacitance as taught by Saeki to broaden the operating range of phase adjustment would have been obvious to one of ordinary skill in the art at the time of the invention since Saeki teaches that this particular delay circuit would provide the capability of allowing performing coarse period adjustment in advance *(see Saeki, col. 2, lines 1-7).*

Allowable Subject Matter

9. Claims 8-13 are allowed.

10. Claims 3-4, 15, 19, 21 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest:

a) The phase blending circuit, in which the at least one transistor comprises a plurality of transistors having different dimensions, as called for in claim 3;

b) A phase blending circuit having a control input for disabling the current source when a late phase signal trailing the early phase signal is asserted, in combination with the remaining claimed limitations, as called for in claim 8;

c) The delay locked loop circuit, in which the control logic is further configured to:

- determine if the input and output signals are aligned within an accepted tolerance,
- if not, modify the one or more control signals to couple a different one or more of the delay elements to the common output node; and
- repeat steps (a)-(b) until the input and output signals are aligned within the

accepted tolerance,

as called for in claim 15;

d) The DRAM device, in which the one or more delay elements comprise a plurality of transistors having different dimensions, as called for in claim 19;

e) The DRAM device, in which the plurality of capacitors are of the same type as capacitors utilized in the memory elements, as called for in claim 21; and

f) The method for generating a phase signal further comprising coupling the late signal to a control input of the current source to disable the current source when the late signal is asserted, as called for in claim 23.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh M. Nguyen
Examiner
Art Unit 2816

LMN